Amendments to the Specification:

Please amend paragraph [0009] to read as follows.

[0009] As an alternative to sending data off-chip, attempts have been made to capture certain state data on chip, thereby reducing the problems of interfacing slower speed test equipment with high-speed devices. In this approach, ~~history buffers, and even on-chip logic analyzers (OCLA) are~~ a history buffer or an on-chip logic analyzer (OCLA) of one type or another is provided to acquire and store event and/or time sequenced data on the chip itself. In the past, to the extent that designers sought to incorporate memory onto the chip for debug and test purposes, dedicated memory devices (usually RAM) were used. Thus, in prior art designs that attempted to capture debug and test information on-chip, a dedicated memory structure was incorporated into the chip design solely to store data for the debug and test modes. The problem with this approach, however, is that it requires the allocation of a significant amount of chip space to incorporate such dedicated memory devices, and these memory devices, while used extensively during the design and development phase of the chip, add little or nothing to the performance of the chip once it is released into production. Thus, the inclusion of dedicated memory space on the chip represents an opportunity cost, and means that functionality and/or performance is sacrificed to include this dedicated memory on the chip. Consequently, the inclusion of memory for debug purposes, while helpful in the debug and test phase, is generally viewed as undesirable because of the accompanying loss of performance and functionality that must be sacrificed. If a dedicated memory device is included on the chip, system designers normally require that such a memory be very small in size to minimize the cost increase (silicon cost is an exponential function of area, and memories are large structures), as well as the performance and functionality loss that accompanies the inclusion of such a dedicated memory. As the size of the dedicated memory becomes smaller, so too does the prospect that the state information stored in the dedicated memory will be sufficient to assist in the debug process. Thus, as the dedicated memory space becomes smaller, so too does the probability that useful debug data will be captured. In relative terms, the

largest dedicated on-chip memories typically are incapable of storing very much data.

Please amend paragraph [0035] to read as follows:

[0035] Referring initially to Figure 1, the present invention constructed in accordance with the preferred embodiment generally comprises an integrated circuit 100 that includes ~~an on-chip logic analyzer 125~~ one or more on-chip logic analyzers 125 coupled to an on-chip memory device 150. In accordance with the preferred embodiment, the on-chip memory device 150 comprises an on-chip cache memory, and the integrated circuit comprises a processor. Various other devices may reside on the processor, including without limitation a memory controller (not shown) that controls accesses to a system memory (not shown), an I/O interface (not shown), and various other logical devices that interface with other components normally implemented in a computer system. In addition, the processor may be designed to operate in a multiple processor environment, and thus may include one or more interfaces for coupling to other processors in a computer system.